

	Hits	Search Text	DBs	Time Stamp
1	2	("5150276").PN.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/18 09:15
2	6	("4686000" "4849854" "4951175" "5053351" "5077688" "5081559").PN.	US- PGPUB; USPAT; USOCR	2005/04/08 15:06
3	31	("5081559").URPN.	USPAT	2005/04/08 15:09
4	71	("5150276").URPN.	USPAT	2005/04/08 15:24
5	2	("20030166318") .PN.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/18 09:16

	L #	Hits	Search Text	DBs	Time Stamp
1	L3	11194	double near4 capacitor	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 08:56
2	L4	1672	3 and dielectric	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 08:57
3	L5	614	4 and bottom and top	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 08:57

	L #	Hits	Search Text	DBs	Time Stamp
4	L6	539	5 and (plug or contact)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 08:57
5	L7	400	6 and cell	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 08:57
6	L8	384	7 and ((@ad<"20030728") or (@rlad<"20030728"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 09:00

	L #	Hits	Search Text	DBs	Time Stamp
7	L9	249	capacitor near4 "cell dielectric"	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 09:01
8	L10	39	second near4 9	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/18 09:01

DOCUMENT-IDENTIFIER: US 20050035392 A1

TITLE: Double-sided capacitor structure for a
semiconductor device and a method for forming the structure

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Abstract Paragraph - ABTX (1):

A method used to manufacture a semiconductor device comprises providing a first conductive container capacitor top plate layer and etching the first conductive container capacitor top plate layer to form a plurality of openings therein. Subsequently, a container capacitor bottom plate layer is formed within the plurality of openings in the top plate layer such that the bottom plate layer defines a plurality of openings. A second conductive container capacitor top plate layer is formed within the plurality of openings in the bottom plate layer. The first conductive container capacitor top plate layer is electrically coupled with the second conductive container capacitor top plate layer. The first and second conductive container capacitor top plate layers and the container capacitor bottom plate layer form a plurality of container capacitors. A structure resulting from the method is also disclosed.

Title - TTL (1):

Double-sided capacitor structure for a semiconductor device and a method for forming the structure

Continuity Related Application Date - RLFD (2):

20020517

Summary of Invention Paragraph - BSTX (2):

[0002] This invention relates to the field of semiconductor manufacture and, more particularly, to a double-sided capacitor structure and a method for forming the structure.

Summary of Invention Paragraph - BSTX (6):

[0005] The FIG. 1 structure is subjected to an anisotropic etch which removes the exposed portions of the BPSG layer to form a patterned BPSG layer which provides a base dielectric having a recess for the container capacitor. During this etch the polysilicon pads 28 and possibly a portion of TEOS capping layer 24 are exposed as depicted in FIG. 2. The remaining photoresist layer is stripped and any polymer (not depicted) which forms during the etch is removed according to means known in the art to provide the FIG. 3 structure.

Summary of Invention Paragraph - BSTX (8):

[0007] Next, the BPSG 32 is partially etched with an etch selective to polysilicon (i.e. an etch which minimally etches or, preferably, doesn't etch polysilicon) to result in the structure of FIG. 6. At this point in the process the polysilicon storage nodes 40 are only minimally supported. The bottom plates 40 in the FIG. 6 structure each comprise a first region 60 which defines a recess, and a second region 62 which defines an opening to the recess, with the first and second regions being continuous, each with the other. In other words, the bottom plate 40 of FIG. 6 defines a receptacle having a rim 62 which defines an opening to the interior of the receptacle. The regions 60, 62 form vertically-oriented sides of the bottom plate, and the sides are electrically-coupled by a horizontally-oriented bottom 64.

Summary of Invention Paragraph - BSTX (10):

[0009] After performing the conversion of the smooth polysilicon to HSG polysilicon, a cell dielectric layer 80, for example a layer of high-quality cell nitride, a polysilicon container capacitor top plate 82, and a planar oxide layer such as BPSG 84 are formed according to means known in the art to result in the FIG. 8 structure. Subsequently, wafer processing continues

according to means known in the art.

Summary of Invention Paragraph - BSTX (11):

[0010] One problem which can result during the process described above is flaking of the HSG polysilicon from the storage node 70 as depicted in FIG. 9. These loose portions 90 are conductive and thus, when they break off and contact two adjacent conductive structures, can short the structures together and result in a malfunctioning or nonfunctioning device. Typically, the greatest number of such defect occurs at the top of the storage plates. This may occur as these ends are not protected by adjacent structures. This may also occur because as wafer processing continues the tops are the most likely portion of the storage plate to be contacted during a CMP or other step, and also incur the highest stresses.

Summary of Invention Paragraph - BSTX (16):

[0014] The present invention provides a new method which, among other advantages, reduces problems associated with the manufacture of semiconductor devices, particularly problems resulting during the formation of double-sided capacitor structures (i.e. capacitor structures having the capacitor top plate formed on two sides of the bottom plate, the inside and the outside of the container, as depicted in FIG. 8). In accordance with one embodiment of the invention an opening is provided in an oxide layer and a first continuous polysilicon layer is formed within the opening. The first polysilicon layer is planarized, for example using a mechanical or chemical mechanical polishing (CMP) process. The first polysilicon layer, which will form a portion of the capacitor top plate, is then etched to form a plurality of recesses therein.

Summary of Invention Paragraph - BSTX (17):

[0015] After forming the plurality of recesses in the first polysilicon

on silicon nitride ($\text{Si}_{3.4}\text{N}_{4.8}$), includes the use of $\text{C}_{4.8}\text{F}_{8.2}$, argon, and O_2 at a pressure of about 30 millitorr and a power of 1500 watts in a reactive ion etcher. In the alternative to using the two etches as described above, one for the first top layer 130 and a second for dielectric layer 118, a single anisotropic etch can be performed which removes layer 130 and layer 118 selective to layer 116.

Detail Description Paragraph - DETX (11):

[0037] Etch stop layer 116 therefore allows etching of materials with different etch rates (the first top plate layer 130 and dielectric layer 118), or different thicknesses, without over etching an underlying layer. An alternative would be to omit the formation of etch stop layer 116, then etch layer 130 with an etch which removes polysilicon 130 selective to dielectric 118. Subsequently, after removing the thickness of layer 130 to expose layer 118 underneath, an etch is performed which removes dielectric 118 selective to the material of layer 28 and 115. This would require an etch which is highly selective to prevent etching of layers 28 and 115 during an extended etch of dielectric 118 to expose pad 115.

Detail Description Paragraph - DETX (13):

[0039] After forming the FIG. 16 structure a first layer of cell dielectric 170 and a capacitor bottom plate seed layer 172 are formed as depicted in FIG. 17. A cell dielectric layer 170, such as cell nitride, can be formed according to means known in the art. A polysilicon bottom plate seed layer 172 having a target thickness of between about 50 .ANG. and about 150 .ANG. may be formed using plasma enhanced chemical vapor deposition (PECVD) techniques. For example, silane gas (SiH_4) is introduced as a silicon source into a deposition chamber at a flow rate of between about 400 sccm and about

600 sccm
along with phosphine (PH.sub.3) at a flow rate of between about 5
sccm and
about 15 sccm at a temperature of between about 500.degree. C. and
about
600.degree. C. for a duration of between about 2.5 minutes and about
15
minutes. Using this process the preferred material is formed at a
rate of
between about 10 .ANG./min to about 20 .ANG./min. As the layer forms
the
PH.sub.3 flow rate may be decreased to 0 sccm over a period of about
10 seconds
as the layer approaches about half its final thickness. This forms a
layer 172
of between about 50 .ANG. and about 150 .ANG. thick.

Detail Description Paragraph - DETX (14):

[0040] Next, the first cell dielectric layer 170 and bottom plate
seed layer
172 are removed from horizontal surfaces of the FIG. 17 structure
using a
spacer etch which etches the seed layer at a slower rate than it
etches the
dielectric to result in the etched nitride 170 and polysilicon as
depicted in
FIG. 18. A spacer etch is also known to etch horizontal surfaces at
a faster
rate than vertical surfaces. This etch forms spacer structures from
the bottom
plate seed layer 172, and may partially etch the first top plate
layer 130.
FIG. 18 further depicts a planar photoresist layer 180 formed after
the spacer
etch. A CMP step is performed on the FIG. 18 structure to result in
the
structure of FIG. 19 which has a planar upper surface.

Detail Description Paragraph - DETX (16):

[0042] After forming the FIG. 21 structure the polysilicon bottom
plate seed
layer 172 may, optionally, be converted to hemispherical silicon
grain (HSG)
polysilicon 220 as depicted in FIG. 22. This step may be performed
using
disilane gas (Si.sub.2H.sub.6) in a CVD system. The disilane gas is
decomposed
into silicon radicals, then nucleation is performed and the smooth
polysilicon
is converted to HSG silicon. After converting the seed layer to HSG

220, a second cell dielectric layer 222 is formed over exposed surfaces according to means known in the art.

Detail Description Paragraph - DETX (17):

[0043] Prior to converting the bottom plate seed layer to HSG polysilicon the seed layer may not actually contact pads 28, 115. FIG. 23 depicts detail of the FIG. 21 structure comprising pad 28, first cell dielectric layer 170 and seed layer 172. After converting the seed layer to HSG polysilicon, however, seed layer 172 expands to contact 28 and make electrical contact therewith as depicted in FIG. 24. Depending on the doping, pad 28 may also have some slight conversion to HSG during the conversion of the seed layer to HSG 220 as depicted in FIG. 24.

Detail Description Paragraph - DETX (18):

[0044] FIG. 25 depicts detail of the upper surface of the FIG. 22 structure. As a wet etch of the bottom plate layer with HF and TMAH as described above removes dielectric at a slower rate than it etches polysilicon, an upper portion of the first cell dielectric layer 170 extends above an upper portion of the bottom plate layer 220 and above an upper portion of first top plate layer 130 which is etched after removal of the horizontal portions of the first cell dielectric layer 170 during the etch between FIG. 17 and FIG. 18. If the upper portions of the first cell dielectric layer 170, bottom plate layer 220, and first top plate layer 130 were at the same level, polysilicon layers 220 and 130, portions of the bottom capacitor plate and top plate respectively, would be separated only by the thickness of the first cell dielectric layer 170. Forming a protruding second cell dielectric layer 222 as depicted "seals" the bottom plate layer 220 and electrically isolates it during operation of the completed device from the first top plate layer 130. Thus leakage of

a charge
stored on a capacitor comprising the first top plate layer 130 and
bottom plate
220 is more resistant to charge leakage between layers 130 and 220
than if the
protruding portion of the nitride 170 was not formed.

Detail Description Paragraph - DETX (19):

[0045] Referring to FIG. 26, after converting bottom plate 220 to
HSG and
forming the second cell dielectric layer 222, a patterned second
capacitor top
plate layer 260, for example a polysilicon layer between about 150
.ANG. and
about 5,000 .ANG. thick, is formed according to means known in the
art. Layer
260 is formed over the majority of the array, and in this embodiment
is not
formed over a portion of at least one first top plate layer portions.
As
depicted in FIG. 26 the first 130 and second 260 capacitor top plate
layers in
this embodiment are not yet electrically connected. However, various
process
modifications may allow for their coupling upon formation of layer
260. The
present method describes various additional steps to electrically
connect the
two layers as described below. Further, FIG. 26 depicts a conductive
plug 262
formed in the periphery concurrently during formation of the
capacitor
structures in the array, and is formed from layer 260. Formation of
plug 262
is not required for the practice of the invention, but is depicted to
demonstrate that concurrent processing of container capacitors in the
array and
conductive plugs in the periphery is possible and may be preferred to
minimize
mask steps.

Detail Description Paragraph - DETX (20):

[0046] In the present embodiment, subsequent to forming the FIG.
26
structure, a planar dielectric layer 270 and a patterned photoresist
layer 272
are formed as depicted in FIG. 27 according to means known in the
art. The
photoresist layer exposes the dielectric layer 270 at opening 274 and
at

3. The semiconductor device of claim 2 further comprising the second cell dielectric layer contacting each contact pad.

Claims Text - CLTX (5):

4. The semiconductor device of claim 1 further comprising a conductive strap which contacts both the first and second conductive capacitor top plate layers to electrically connect the first and second conductive capacitor top plates together.

Claims Text - CLTX (6):

5. The semiconductor device of claim 1 wherein a height of the second conductive capacitor top plate layer is greater than a height of the first conductive capacitor top plate layer.

Claims Text - CLTX (7):

6. The semiconductor device of claim 1 further comprising an upper portion of the first cell dielectric layer extending above an upper surface of the first conductive capacitor top plate layer and of an upper surface of each conductive capacitor bottom plate.

Claims Text - CLTX (8):

7. The semiconductor device of claim 6 further comprising the second cell dielectric layer contacting the first cell dielectric layer at the upper portion of the first cell dielectric layer.

Claims Text - CLTX (9):

8. The semiconductor device of claim 1 wherein the bottom plate is a hemispherical silicon grain (HSG) layer.

Claims Text - CLTX (10):

9. A semiconductor device comprising: a storage capacitor comprising: a first capacitor top plate layer having a plurality of openings therethrough; a plurality of capacitor bottom plates, with each bottom plate located at least partially within one of the plurality of openings in the first capacitor top

plate layer, wherein each bottom plate comprises a recess therein; a second capacitor top plate layer partially located within each of the plurality of openings in the first capacitor top plate layer and within each recess of each bottom plate and having a portion located over each capacitor bottom plate and a portion located over the first capacitor top plate layer; and a conductive strap which contacts both the first and second capacitor top plate layers.

Claims Text - CLTX (11):

10. The semiconductor device of claim 9 further comprising: a first cell dielectric layer which separates the first top plate layer from each bottom plate; and a second cell dielectric layer which separates each bottom plate from the second capacitor top plate layer and which separates the first capacitor top plate layer from the second capacitor top plate layer.

Claims Text - CLTX (12):

11. The semiconductor device of claim 10 further comprising the conductive strap contacting the second cell dielectric layer.

Claims Text - CLTX (13):

12. The semiconductor device of claim 9 wherein the bottom plate is a hemispherical silicon grain (HSG) layer.